AXUS TECHNOLOGY

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WAFER BONDING PROCESS
Application Note

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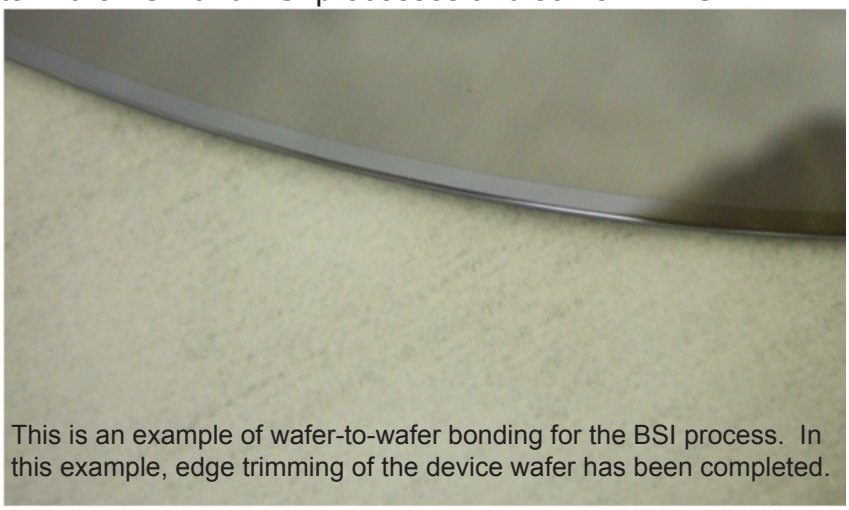
This paper addresses the topic of the various bonding techniques common to the semiconductor industry and also common in applications such as MEMS, MOEMS, TSV, BSI, and others. Bonding is commonly used in FEOL operational steps as wafer-to-wafer bonding provides strength if the device wafer is to be thinned to ultra-thin dimensions. Bonding is also an integral BEOL step and is commonly done as a chip-to-wafer, chip-to-chip, or chip-to-cover (protective covering or sealing) operational step. This paper is primarily devoted to FEOL (whole wafer) applications.

Wafer Bonding Applications

Precision bonding of a wafer to a substrate in the TSV and BSI processes and some MEMS processes is done primarily for the purpose of providing strength and wafer safety during follow-on process steps and handling. Device wafers in the TSV and BSI processes are put through an ultra-thin grinding process which reduces the device wafer thickness to 50 µm for TSV and even thinner for BSI. Without a supportive substrate, silicon wafers this thin will not survive follow-on multi-step processing. As a part of the bonding procedure, it is common for both the device wafer and the "carrier" substrate to pass through one or more CMP steps for planarization and surface smoothness preparation.



This is an example of wafer-to-wafer bonding for the BSI process. In this example, edge trimming of the device wafer has been completed.

In wafer-to-wafer bonding for applications such as semiconductor ICs, MEMS, MOEMS, TSV, and BSI, several questions must be considered when bonding methods are being chosen.

1. Is a permanent or a temporary bond required?
2. What is the cleanliness requirement?
3. How smooth do the surfaces have to be?
4. How planar do the surfaces have to be?
5. What is the requirement for post-bond alignment (sub-micron?)
6. Will the differences in the Coefficient of Thermal Expansion of the wafer and substrate have a negative effect on the strength and effectiveness of the bond?
7. What is the shortest bonding time that can be achieved?
8. What is the shortest debonding time that can be achieved?
9. What is the minimum edge exclusion that is required for this application?
10. Is edge protection critical?
11. What is the most effective bonding method to achieve the required compatibility with the topo graphical surfaces of the wafer against the substrate to eliminate voids?
12. If the bond is to be temporary, what is the best release method?
13. If the bond is to be temporary, what is the easiest and quickest yet most effective clean-up method post-release?

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Axus Technology has the experience and expertise to provide bonded wafers using various industry-standard methods including:

- Surface Bonding
  - Direct Hydrophilic
  - Direct Hydrophobic
  - Plasma Activated
  - Wax
  - Tape
- Metallic Layer Bonding
  - Eutectic bonding
  - Reactive bonding
  - Thermo-compression bonding
- Insulator Layer Bonding
  - Adhesive bonding - (gluing)
  - Anotic – (electrostatic sealing)
  - Glass Frit – (spin on or by silk-screen printing)

The Axus Technology's Solution

Axus Technology offers a variety of wafer bonding process techniques including: temporary wax-on and tape-on bonding, permanent wafer bonding and enhanced temporary bonds where follow-on processing requires stronger bonding of the substrates. Many companies now are asking Axus Technology to take the lead by managing a combination of these bonding services along with other world-class capabilities available at Axus Technology such as:

- Edge profiling
- Precision grinding
- Precision polishing and CMP
- Edge trimming
- Wafer ultra-thinning
- Post-process wafer cleaning
- Metrology services

The combination of these special capabilities makes Axus Technology the one-stop central source for a wide range of process services for advanced chip and device manufacturing.

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Conclusions

In certain advanced wafer applications such as TSV and BSI, and certain MEMS applications which can benefit from, or even require the support of a carrier substrate to protect the device wafer in thin wafer processing, customers soon understand that bonding their device wafers to support-substrates can provide the needed protection. The type of bonding that is chosen is based upon the application and the materials involved. Superior bonding results are dependent upon upstream processing steps such as superior precision grinding, edge treatments such as profiling and trimming, along with Chemical Mechanical Polishing (CMP), and post-process cleaning. Relying on one supplier, such as Axus Technology to be responsible for all of these process steps mitigates the customer's risk and shortens the overall processing time.

How Axus Technology Can Help You

FOR PROCESS SERVICES: Axus Technology's Process Services Department has the required equipment and expertise available to perform a number of critical process steps including wafer bonding on a contractual basis on your wafer substrates.

Please contact us to learn more about this and our many other precision polishing, grinding, and cleaning process capabilities.

About Axus

Axus Technology provides surface processing solutions for a range of semiconductor, MEMS, substrate, and related technologies. Along with providing parts and support services for existing tools, Axus Technology delivers economical leading-edge equipment and process solutions that are precisely configured for end-user applications.

Based in Chandler, Arizona, Axus Technology operations include a fully equipped development and foundry processing facility, as well as design, manufacture, and service operations. For more information visit our website at www.AxusTech.com.